CONTENTS

1 References, Abbreviations and Definitions

1.1 References

Ref.	Document Title	Registration Number
[1]	Package Type 5	M4939

1.2 Abbreviations

TBD	To Be Determined
TBC	To Be Confirmed
NA	Not Applicable
FSI	Full Scale Input
FSO	Full Scale Output
SPI	Serial Peripheral Interface
ASIC	Application Specific Integrated Circuit
ESD	Electro Static Discharge
MSB	Most Significant Bit
LSB	Least Significant Bit
NC	Not Connected
OTP	One-Time Programmable Read Only Memory

1.3 Definitions

- The min. and max. specifications reflect 4σ values over the complete operating temperature and supply voltage ranges unless otherwise noted.
- 1g = 9.80665 m/s^2 .
- Voltages are referenced to AV_{SS}/V_{SS} unless otherwise specified (AV_{SS} is assumed shorted to V_{SS}).

2 Description

The SAR10 is an angular rate sensor designed for automotive rollover detection. The purpose of the sensor is to convert a rotation around the sensitive axis to digital data sample values representing the rotational velocity at any point in time.

The SAR10 consists of a sensor die and an ASIC housed in a dual-in-line transfer molded package for surface mounting.

The principle of operation is based on the Coriolis force. The mass of the sensor element is excited with an angular vibration around one axis. An input rotation results in a detection vibration around the axis normal to the excitation axis and the input axis.

An SPI interface enables communication between the application and the SAR10. The angular rate data output from SAR10 is a 10-bit 2's complement data word. The 8 MSBs of an angular rate data sample are mapped to the 8 bit response of the RARH (read angular rate high byte) command. The 2 LSBs of the sample are mapped to the 2 LSBs of the 8 bit response of the RARL (read angular rate low byte) command. The RARH command latches the 2 LSBs of a sample such that a RARH, RARL command sequence guarantees bits from the same angular rate sample. The "unused" 6 MSBs of the response from the RARL command is always a '010101' bit pattern, providing a mechanism for detecting "stuck at" errors in the communication between SAR10 and the application.

Note that when using the RARH and RARL SPI commands to read angular rate data, due to the serial nature of the SPI bus, the 8 bit data word requested by one SPI command (number 'N') is provided at the time of the following command (number 'N+1').

The response to the RARH and RARL commands will be the Error Code if the angular rate sample data is not valid. The Error Code is a bit pattern, which cannot be confused with real rate data, see 7.13.

The sensor is calibrated by means of a set of internal OTP bit fuses.

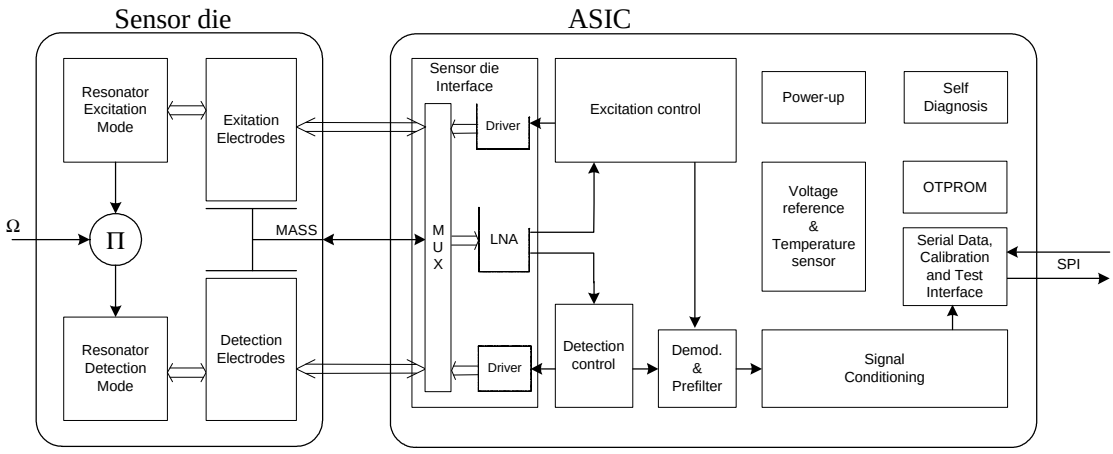

Figure 1 - SAR10 block diagram

3 Operating Conditions

Characteristics	Symbol	Note	Specifications			
			Min	Nom	Max	Units
3.1 Operating range	Ω_{FSI}		±250			°/s
3.2 Dynamic overload, angular rate	Ω_{OVL}	1,7	±1200			°/s
3.3 Dynamic overload, shock		1,6,7	±500			g
3.4 Supply voltage	V_{DD}, AV_{DD}	2	4.45	5.0	5.5	V_{DC}
3.5 Current consumption		3			17	mA
3.6 Excitation mode resonance frequency	f_{EXC}	4,7	7.9	9.4	10.9	kHz
3.7 Internal master clock	f_{MCLK}	5,7	7.6	8.0	8.4	MHz

Note 1: The PRCEN command will have to be issued to revert to normal functionality. Also see 10.2.
Note 2: Both digital (V_{DD}) and analog (AV_{DD}) supply voltage.
Note 3: Total current consumption from both analog and digital supply.
Note 4: Detection frequency is electrostatically tuned during calibration to match the excitation frequency.
Note 5: After calibration.
Note 6: Shock below 500g/1ms will never result in an error condition. For shocks not resulting in an error condition the shock sensitivity is <0.3°/s/g_{peak}. Transient pulses containing frequencies >26kHz may cause excitation of resonant modes creating larger effects.
Note 7: By design. The values are specified in IBS (sensor die specification).

4 Environmental Requirements

Characteristics	Symbol	Note	Specifications			
			Min	Nom	Max	Units
4.1 Operating temperature	T_{OPER}		-40		+90	°C
4.2 Storage temperature			-40		+125	°C
4.3 Temperature gradient		1			±5	K/min

Note 1: By design.

5 Absolute Maximum Ratings

Prolonged exposure to absolute maximum ratings may affect the performance and/or reliability of the device.

Characteristics	Symbol	Note	Specifications			
			Min	Nom	Max	Units
5.1 Supply voltage	V_{DD}, AV_{DD}		-0.5		7.0	V_{DC}
5.2 Input voltage, any pin			-0.5		V_{DD}+0.5	V_{DC}
5.3 Input transient current, any pin					±100	mA
5.4 Short circuit immunity to V_{DD}/AV_{DD} or V_{SS}/AV_{SS}, any output					10	min
5.5 ESD voltage immunity, Human Body Model, any pin		1			2000	V
5.6 ESD voltage immunity, Machine Model, any pin		2			200	V
5.7 Mechanical shock immunity		3			5000	g
5.8 Ambient temperature		4	-40		+125	°C

Note 1: According to AEC-Q100-002 – REV-C.
Note 2: According to AEC-Q100-003 – REV-E.
Note 3: According to MIL-STD 883E.
Note 4: Ambient temperature with power on sensor.

6 Mechanical Characteristics

6.1 Package

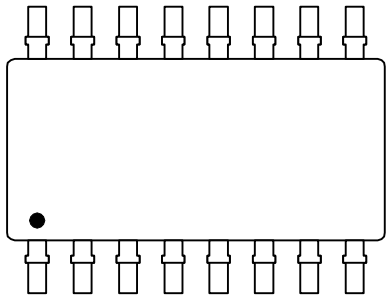

Figure 2 – Sensor pin out (dot marks pin no. 1)

Characteristics	Symbol	Note	Specifications
6.2 Package type			Plastic moulded SOIC
6.3 Number of pins			16
6.4 Outline drawing			See ref. [1].

6.5 Pin assignments

Pin Number	Name	Type	Direction	Note	Function
1	SCLK	Digital	Input		SPI clock
2	LOAD	Digital	Input		SPI load
3	V_{SS}	Power	-	1	Digital Ground
4	AV_{SS}	Power	-	1	Analog Ground
5	NA	-	-	2	Connect to ground in application
6	REFV	-	-		Internal voltage reference. For details see Chapter 9
7	NC	-	-	2	No internal connection
8	NC	-	-	2	Lead frame
9	NC	-	-	2	Lead frame
10	NC	-	-	2	No internal connection
11	NA	-	-	2	Connect to ground in application
12	NA	-	-	2	Connect to ground in application
13	AV_{DD}	Power	-	1, 3	Analog +5V supply voltage
14	V_{DD}	Power	-	1, 3	Digital +5V supply voltage
15	MOSI	Digital	Input		SPI data input
16	MISO	Digital	Output	4	SPI data output

Note 1: To be connected externally.
Note 2: To minimize noise levels connect to AV_{SS}/V_{SS}.
Note 3: To minimize noise connect 100nF low ESR decoupling capacitor between pin and ground, as close to the pin as possible.
Note 4: This signal is tri-stated when LOAD is logical '1' (> $0.7V_{DD}$).

6.6 Sensor Axes Definitions and Sensitive Direction

The arrow around the X-axis indicates the rotational direction for positive angular rate. The X-axis is normal to the figure plane; its positive direction outwards. For details see ref. [1].

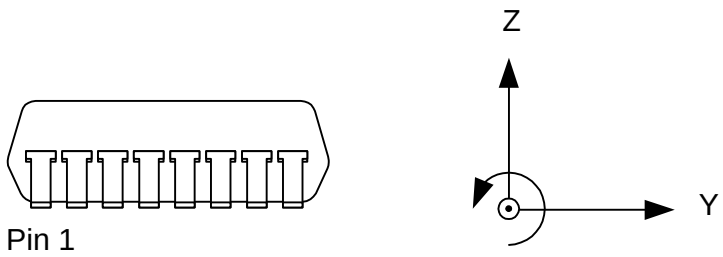

Figure 3 - Axes Definitions and Sensitive Direction

6.7 Product markings

See ref. [1].

7 SPI Serial Data Interface

Serial data communication with the application is through an SPI interface.

7.1 Signal Definitions and Characteristics

The SPI interface consists of 4 signals – MOSI, MISO, SCLK and LOAD:

Name	Signal Description
MOSI	**Master Out, Slave In.** After a negative edge on LOAD, 8-bit command is shifted in on MOSI, clocked by SCLK (MSB first).
MISO	**Master In, Slave Out.** Output from previous command is stored in a Data Register. At a negative edge on LOAD, the content of the Data Register is loaded to the Data Output Register. While command byte is shifted into the Command Register, Data Output is shifted out on MISO (MSB first).
LOAD	**Chip Select/Transfer Start Strobe.** As long as LOAD=1, the MISO output is tri-stated. A negative edge on LOAD initiates SPI transfer. The new command is executed after a positive edge on LOAD. If a positive edge occurs on LOAD before at least 8 bits are shifted in on MOSI, the command will be ignored.
SCLK	**Serial Data Clock.** MOSI is read on the positive edge of SCLK, and MISO is shifted out on the negative edge of SCLK.

Characteristics	Symbol	Note	Specifications			
			Min	Nom	Max	Units
7.2 High ('1') level	V_H	2	$0.7V_{DD}$			V
7.3 Low ('0') level	V_L	2			$0.3V_{DD}$	V
7.4 Input rise time	t_{rI}	2			$1/(20f_{SCLK})$	s
7.5 Input fall time	t_{fI}	2			$1/(20f_{SCLK})$	s
7.6 Output fall time	t_{PHL}	1,2			8.5	ns
7.7 Output rise time	t_{PLH}	1,2			8.6	ns
7.8 Output enable delay	t_{PHZ} t_{PLZ} t_{PZH} t_{PZL}	1,2			1.2 0.97 8.4 8.2	ns
7.9 Data rate	f_{SCLK}	3			8.5	Mbits/s
7.10 Capacitive load, MISO	C_{MISO}	2			100	pF

Note 1: With load of 100pF connected to V_{SS}.
Note 2: Characteristic based on proven STKM5006 library I/O cell performance.
Note 3: By design.

7.11 SPI Commands

Name	Command	Address	Output	Description	Note
Read Commands					
RARH	10000000	-	dddd dddd	Read Angular Rate, High Byte	2
RARL	10001111	-	0101 01dd	Read Angular Rate, Low Byte	
RSR	10110100	-	Status byte	Read status register	
High Pass Filter Commands					
HPINI	11000100	HPFININ level	1000 0000	Initialize High pass filter	4
SafeGuard Commands					
SGDIS1	01001110	11010111	1000 0000	SafeGuard Disable Command 1	1
SGDIS2	01100011	01010000	1000 0000	SafeGuard Disable Command 2	
SGDIS3	00010010	10101000	1000 0000	SafeGuard Disable Command 3	
SGEN	01010101	-	1000 0000	SafeGuard Enable Command	
Error Handling Commands					
PRCEN	10101010	-	1000 0000	Re-enable signal processing after error condition	3

Other commands are available for test modes used during calibration and programming.

Note 1: The three SafeGuard disable commands MUST be issued in the -1,-2,-3 sequence, and with the addresses shown. Any in-between commands or incorrect addresses will reset the Safeguard Disable sequence. A single SGEN command re-enables the SafeGuard. The option to disable the SafeGuard is intended as a way for the application to access the HPINI and PRCEN commands, see 10.1 and 10.2.

Note 2: The RARH command latches bits 1 and 0 such that a sequence of RARH first followed by RARL guarantees bits from the same Angular Rate sample.

Note 3: In case of a recoverable error condition, issuing this command re-enables continued angular rate readout. Note that for this command to function the SafeGuard must be disabled. Also see 10.2.

Note 4: This command initializes the High pass filter. Note that for this command to function the SafeGuard must be disabled.

7.12 Timing diagram

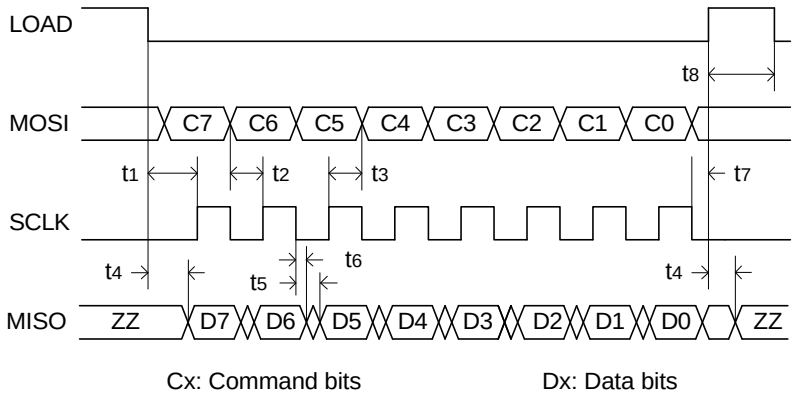

Figure 4 - SPI interface signal timing diagram

For commands that need an address, the address byte is shifted in prior to the command byte.

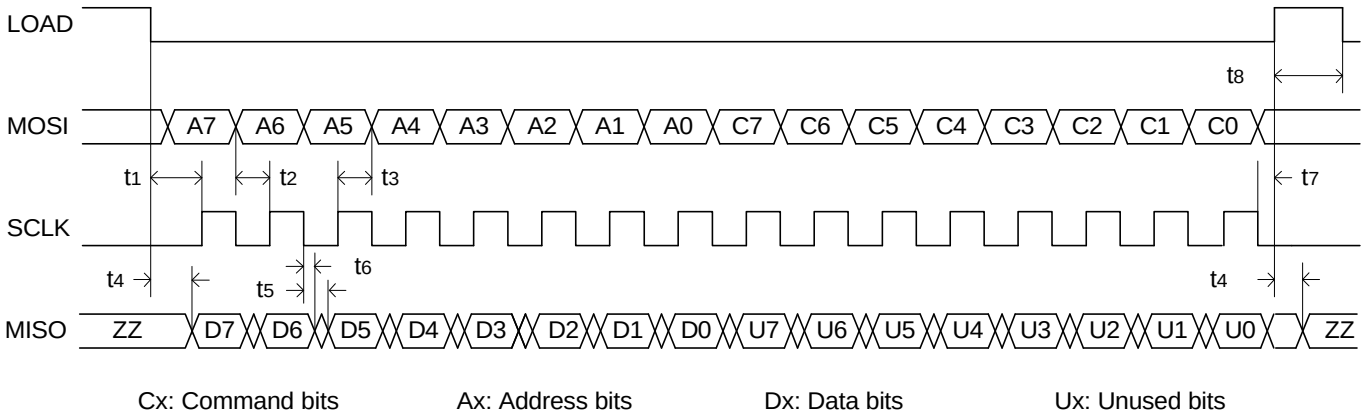

Figure 5 - SPI interface signal timing diagram for command with address byte

Symbol	Parameter (time from ...)	Specification			Note
		Min	Max	Units	
t_1	... falling edge of LOAD to the first rising edge of SCLK	10		ns	2
t_2	... stable data at MOSI to rising edge of SCLK (MOSI data setup time)	10		ns	2
t_3	... rising edge of SCLK to new data at MOSI (MOSI data hold time)	10		ns	2
t_4	... falling edge or rising edge of LOAD to active or high impedance state of MISO		20	ns	2
t_5	... falling edge of SCLK to stable new data at MISO (MISO data output delay)		20	ns	2
t_6	... falling edge of SCLK to removal of old data at MISO (MISO data hold time)	0		ns	2
t_7	... last falling edge of SCLK to next rising edge of LOAD	20		ns	2
t_8	... rising edge of LOAD to falling edge of LOAD	527		ns	1,2

Note 1: Minimum 4 internal MCLK cycles = 4 * 1/7.6MHz.
Note 2: By design.

7.13 Error Code

The Error Code is a bit pattern defined as $1000\ 0000_2$. The error code is the output from SAR10 under following conditions:

- SPI response for RARH, RARL commands during start-up.
- If an illegal command is executed.
- If an RARH or RARL command is executed and any of the Status Register flags is a '0'.

Error code is defined to be $10\ 0000\ 0000_2$ as response for either RARH or RARL command. This cannot be confused with valid angular rate data which is limited to the maximum ± 508 LSB.

8 Angular Rate Output

Characteristics	Symbol	Note	Specifications			
			Min	Nom	Max	Units
Angular rate data format						
8.1 Word length				10		bit
8.2 Format				2's complement		
8.3 SPI command(s)				RARH RARL		
8.4 Scale factor				1		LSB/(°/s)
8.5 Full scale signal	$+\Omega_{FSO}$ $-\Omega_{FSO}$	1	High byte 00111110 11000001	Low byte 01010110 01010110	(+250 °/s) (–250 °/s)	
8.6 Zero rate output			High byte 00000000	Low byte 01010100	(0 °/s)	
8.7 Error Code			High byte 10000000	Low byte 10000000		
Accuracy						
8.8 Sensitivity error		1			±6	%
8.9 Non-linearity					±0.3	%FSO
8.10 Noise referred to input		2			1.5	°/s (rms)
8.11 Zero-rate error					±1.6	%FSO
8.12 Zero-rate drift over 100s		8			±1	°/s
8.13 Vibration sensitivity referred to input		6			±0.3	(°/s)/g
8.14 Cross-axis sensitivity referred to input		7			±0.04	(°/s)/ (°/s)
Frequency response		5				
8.15 Sampling rate	f_S		1.8	2	2.2	kHz
8.16 Pass band ripple		4,9			0.2	dB
8.17 Group delay		9			13	ms
8.18 Lower passband cut-off frequency	f_L	3,9	0.007	0.01	0.013	Hz
8.19 Roll-off for f < f_L		9	18	20	22	dB/dec
8.20 Upper passband cut-off frequency	f_H	3,9	45	50	55	Hz
8.21 Roll-off for f > f_H		9	90	100	110	dB/dec
8.22 Attenuation for f > 310 Hz		9	60			dB

Note 1: Measured at f_Ω =2Hz.
Note 2: Integrated over f_L to f_H.
Note 3: -3dB frequency.
Note 4: 1Hz < f < 39Hz.
Note 5:

HP-filter transfer function: $H(z)=\frac{1-z^{-1}}{1-p_0 z^{-1}}, p_0=\frac{1-\frac{f_L}{2f_S}}{1+\frac{f_L}{2f_S}}$ (with nominal f_L and f_S values)

LP-filter transfer function: $H(z)=\frac{b_{01}+b_{11}\cdot z^{-1}+b_{21}\cdot z^{-2}}{1-a_{11}\cdot z^{-1}-a_{21}\cdot z^{-2}}\cdot\frac{b_{02}+b_{12}\cdot z^{-1}+b_{22}\cdot z^{-2}}{1-a_{12}\cdot z^{-1}-a_{22}\cdot z^{-2}}$

a_{11}	1.91064453125E+00	a_{12}	1.829833984375E+00
a_{21}	-9.31640625E-01	a_{22}	-8.40087890625E-01
b_{01}	1.0498046875E-02	b_{02}	7.8125E-03
b_{11}	-1.0498046875E-02	b_{12}	4.8828125E-03
b_{21}	1.0498046875E-02	b_{22}	7.8125E-03

Note 6: Frequencies < 5.4 [kHz]. Stationary vibrations above 5.4 [kHz] hitting resonant modes may cause larger effects. This effect is highly nonlinear.
Note 7: Includes effects caused by mechanical misalignment due to package tolerances. See [1].
Note 8: By design.
Note 9: Guaranteed by theoretical digital filter design and verification (characteristics depends only on master clock frequency, also see 3.8)

9 Power Supply and Start-up

The SAR10 is intended powered by a single +5 volt supply. The device has four pins for power connection: V_{DD}, AV_{DD}, V_{SS} and AV_{SS}. The V_{SS} and AV_{SS} pins shall be connected together on the printed circuit board as close to the device as possible. The same rule applies to V_{DD} and AV_{DD}. A simultaneous power-on of the two supplies is essential to prevent internal latch-up conditions. An external power supply decoupling capacitor is needed. This decoupling capacitor should be a low ESR 100nF capacitor connected to the supply line as close to the V_{DD} and V_{SS} pins (shaded) as possible.

An additional decoupling capacitor is needed between pin 6 (REFV) and V_{SS}. This should also be a low ESR 10nF capacitor connected as close as possible to pin 6 and V_{SS} pin.

The SAR10 ASIC employs a supply voltage surveillance circuit which sets the Status Register flag PRNG_OK to '1' only if AV_{DD} is within a specific range (see 9.7). If outside this range, the PRNG_OK flag is set to '0'.

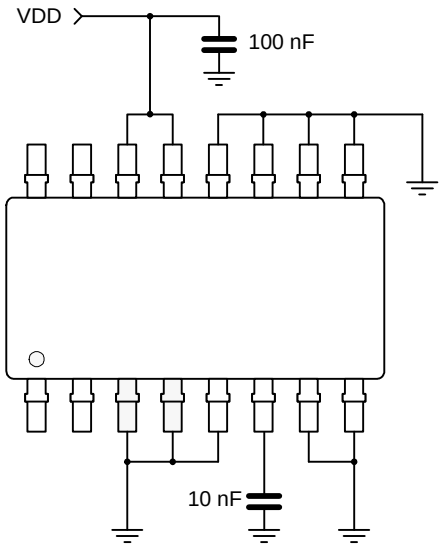

Figure 6 - Power Supply and Decoupling

Characteristic	Symbol	Note	Specifications			
			Min	Nom	Max	Units
9.1 Supply voltage rise time to V_{DD-MIN}	t_D	1	0.001		10	ms
9.2 Start-up time, phase 1	t_{INIT1}	2			0.6	s
9.3 Start-up time, phase 2	t_{INIT2}				1.0	s
9.4 Minimum AV_{DD} for internal RESET	V_{RU}	3, 7			1.0	V_{DC}
9.5 Detectable AV_{DD} glitch	t_G	7	10			ns
9.6 Reset threshold	V_{RESET}	4	2.5		3.5	V_{DC}
9.7 Status Register AV_{DD} OK flag (PRNG_OK) threshold	V_{PRNGH}	5	5.55		5.91	V_{DC}
	V_{PRNGL}		4.2		4.43	
9.8 Reset delay	t_{RSTN}	6, 7	128		208	µs

Note 1: The voltage V_{DD-MIN} is the lower limit for V_{DD} and A_{VDD} as specified in 3.4.
Note 2: The first phase, t_{INIT1}, is defined as the time until the Status Register flag EXC_OK goes to '1' (sensor excitation has stabilized). The second phase, t_{INIT2}, is defined as the fixed delay time from EXC_OK has gone to '1' until the automatic HP Filter initialization is performed. The total SAR10 start-up time is the sum of t_{INIT1} and t_{INIT2}.
Note 3: Internal reset signal is defined for supply voltage above V_{RU}.
Note 4: Internal reset is activated when the supply voltage passes V_{RESET}. The reset threshold has a small hysteresis (approx. 0.1V).
Note 5: The RARH and RARL commands return the Error Code when $AV_{DD} \leq V_{PRNGL}$ or $AV_{DD} \geq V_{PRNGH}$. Also see 10.2 and 7.13.
Note 6: For correct OTP power-down a reset pulse width of minimum 50 µs is needed.
Note 7: By design.

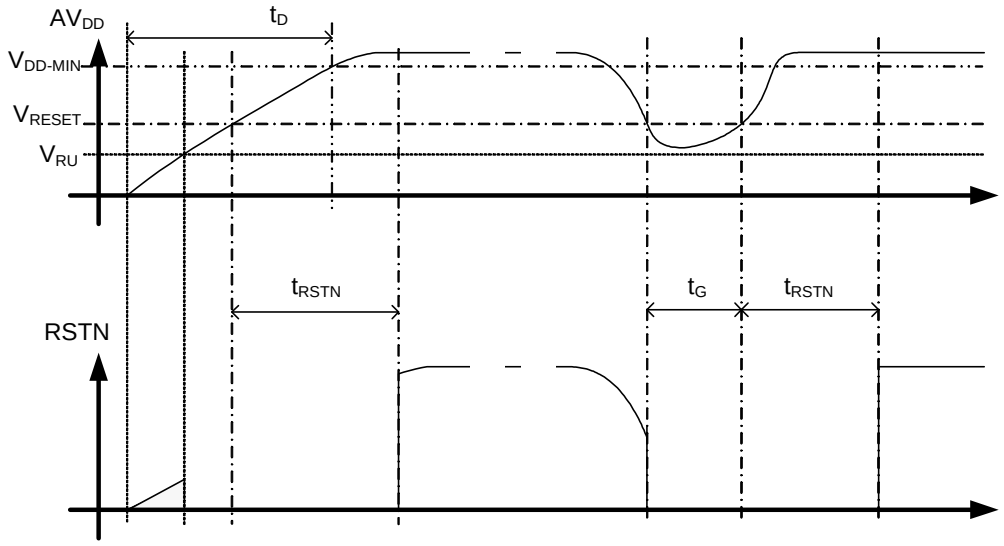

Figure 7 - Power-Up and Power Glitch Reset Timing

10 Application Information

10.1 High Pass Filter (HPF) Initialisation

The SAR10 has an automatic HPF initialisation feature. After the device start-up is completed, the device will initialize the HP filter and start to respond to RARH and RARL commands with real rate data instead of 'Error Code' (also see 7.13)

The High Pass (HP) Filter initialization can be carried out manually by means of the HPINI command. **This is not recommended unless supported by reliable information on device start-up behaviour.** To perform the manual HP filter initialization it is recommended to sample continuously the EXC_OK flag immediately following power-up, and apply the HPINI command at the time EXC_OK goes to '1' **after** a defined delay time. **Note that if the HPINI command is applied before EXC_OK goes to '1' the device will be rendered in a 'recoverable error' state, see 10.2 for more details.**

Please note that the HPINI command action depend on the supplied address. If the address is non-zero, the HP Filter is rendered in a state of continuous initialisation. If the address is zero, the HP Filter is taken out of initialisation mode.

A typical use of the initialisation command would be to issue it with a non-zero address, wait for at least 0.5 ms, and then issue it with a zero address.

Note that for the HPINI command to work the SafeGuard must first be disabled. To resume normal operation after initialization, the SafeGuard must be re-enabled by issuing the SGEN command.

10.2 Status Register and Internal Function Monitoring

Internally in the SAR10 ASIC, 6 error-monitoring functions are employed to make sure an unreliable output angular rate is detected. If any of the monitoring functions detects an error condition the corresponding flag becomes a '0', otherwise a '1'.

The Status Register flags are available to the application via the RSR SPI command.

It is assumed that a flag can signal an error for any length of time. To make sure short "error" ('0') pulses are visible to the application, the '0' pulses are "stretched" in time such that they are at least between 1.5 and 2 ms. Status register shall be read within 1.5ms to not loose this information.

Bit Position	Flag Name	Monitoring function	Recover-able
7	ADC_OK	ADC_OK is '0' if an ADC overflow occurs, otherwise '1'.	Yes
6	SIG_OK	SIG_OK is '0' if an arithmetic overflow or underflow occurs in the digital signal processing, EXCEPT if the signal amplitude exceeds the output range in the final scaling (by the S0INV parameter), otherwise '1'.	No
5	OTPPAR_OK	OTPPAR_OK is '0' if OTP parity check fails, otherwise '1'.	No
4	ATEST_INACTIVE	ATEST_INACTIVE is '0' if an analog test mode is active, otherwise '1'. This monitoring function will not result in any Error Code signalling.	-
3	PRNG_OK	PRNG_OK is '0' if the AV_{DD} voltage is out of range, otherwise '1'.	No
2	DET_OK	DET_OK is '0' if one or both connections to the sensor die detection electrodes is open or if a leakage current is present on one or both electrodes, otherwise '1'.	-
1	EXC_OK	EXC_OK is '0' if the excitation control loop fails to lock on resonance frequency such that the excitation amplitude falls below a critical level, otherwise '1'.	Yes
0	(no name)	Not used. Always '1'.	-

After power-up and until the device start-up is completed the output from the RARH and RARL commands are substituted by the Error Code, see 7.13.

After start-up, if any of the flags (except DET_OK) go to '0' (the internal monitoring functions indicate that the output will not be reliable), the Error Code is the output from the RARH and RARL commands, and also internal digital signal processing is

held. This error signalling continues indefinitely until the device is powered down, or, in case of some of the conditions (see 'Recoverable' in the table above), until the PRCEN command is issued.

For the DET_OK flag, the error signalling continues only as long as the error condition is present, the error signalling latching and holding of internal digital signal processing is not implemented for this flag. Hence this error condition is not classified as recoverable or non-recoverable.

The PRCEN command execution must obey the following algorithm:

1. **Wait until no recoverable error conditions are flagged (polling the Status Register).**
2. **Wait 1 second.**
3. **Execute the SGDIS1, -2 and -3 commands.**
4. **Execute the PRCEN command.**
5. **Execute the SGEN command**

Note that for the PRCEN command to take effect, the Safe Guard must first be disabled by means of the SGDIS1,-2 and -3 commands. To resume normal operation after recovery, the SafeGuard must be re-enabled by using the SGEN command. If, before the Safe Guard was disabled, a non-recoverable error condition existed, the SAR10 ASIC will return to responding with the Error Code to RARH, RARL commands as well as holding internal digital signal processing even after the SGEN command was issued (the error is **non-recoverable**).

Also note that while the SafeGuard is disabled, no error condition will be latched. To ensure maximum SAR10 operational integrity, the Safe Guard should only be turned off briefly (for less than a millisecond).